Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **N. 1OE**
2. **1A0**
3. **N. 2Y3**
4. **1A1**
5. **N. 2Y2**
6. **1A2**
7. **N. 2Y1**
8. **1A3**
9. **N. 2Y0**
10. **GND**
11. **2A0**
12. **N. 1Y3**
13. **2A1**
14. **N. 1Y2**
15. **2A2**
16. **N. 1Y1**
17. **2A3**
18. **N. 1Y0**
19. **N. 2OE**
20. **VCC**

**.095”**

**13**

**12**

**11**

**10**

**9**

**8**

**17 16 15 14**

**4 5 6 7**

**18**

**19**

**20**

**1**

**2**

**3**

**.062”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 x .004”**

**Backside Potential:**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .062” X .095” DATE: 9/7/21**

**MFG: RCA THICKNESS .020” P/N: 54HCT240**

**DG 10.1.2**

#### Rev B, 7/1